AMENDMENTS TO THE CLAIMS

Please cancel claim 3 without prejudice or disclaimer of its underlying subject matter.

1-5. (Canceled)

6. (Previously presented) A semiconductor testing apparatus comprising:

control means adapted to generate a timing signal and an address specifying signal, said timing signal having a test pattern cycle period, the duration of said test pattern cycle period being variable, the rate of modification for said address specifying signal being said test pattern cycle period;

test pattern memory means adapted to store a first test pattern, said first test pattern being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period; and

test pattern generation means adapted to generate an input test pattern signal by combining said first test pattern with said timing signal, a semiconductor device under test receiving said input test pattern signal.

7. (Previously presented) The semiconductor testing apparatus according to claim 6, further comprising:

decision means adapted to detect a failure within said semiconductor device by comparing an output test pattern signal received from said semiconductor device under test with said first test pattern.

8. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said control means is adapted to vary said duration of said test pattern cycle period.

9. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said first test pattern is located at an address within said test pattern memory means.

10. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said semiconductor device is tested during said test pattern cycle period.

11. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said control means receiving set information to generate said timing signal and said address specifying signal, said set information establishing said duration of said test pattern cycle period.

12. (Previously presented) The semiconductor testing apparatus according to claim 11, wherein said control means controls the timing of generation of said first test pattern on the basis of said set information.

13. (Previously presented) The semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is narrowed by varying said set information.

14. (Previously presented) The semiconductor testing apparatus according to claim 11, wherein said test pattern cycle period is widened by varying said set information.

15. (Previously presented) The semiconductor testing apparatus according to claim 6, wherein said test pattern memory means stores a plurality of test patterns, said plurality of test patterns being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said plurality of test patterns being said test pattern cycle period.

16. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed.

17. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

18. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

19. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period only for said first test pattern is widened.

20. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

21. (Previously presented) The semiconductor testing apparatus according to claim 15, wherein said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.

22. (Previously presented) A semiconductor testing method for conducting a test of a semiconductor device comprising the steps of:

generating a timing signal having a test pattern cycle period;

varying the duration of said test pattern cycle period;

generating an address specifying signal, the rate of modification for said address specifying signal being said test pattern cycle period;

storing a first test pattern within test pattern memory means;

outputting said first test pattern from within test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period;

combining said first test pattern with said timing signal to generate an input test pattern signal, a semiconductor device under test receiving said input test pattern signal; and

comparing an output test pattern signal from said semiconductor device under test with said first test pattern.

23. (Previously presented) The semiconductor testing method according to claim 22, further comprising the steps of:

receiving set information to generate said timing signal and said address specifying signal; and

using said set information to establish said duration of said test pattern cycle period.

24. (Previously presented) The semiconductor testing method according to claim 23, wherein said test pattern cycle period is narrowed by varying said set information.

25. (Previously presented) The semiconductor testing method according to claim 23, wherein said test pattern cycle period is widened by varying said set information.

26. (Previously presented) The semiconductor testing method according to claim 22, wherein said test pattern memory means stores a plurality of test patterns, said plurality of test patterns being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said plurality of test patterns being said test pattern cycle period.

27. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is narrowed.

28. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is narrowed.

29. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is narrowed successively from the top pattern address throughout the entire test pattern in order.

30. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period only for said first test pattern is widened.

31. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said first test pattern and for said plurality of test patterns is widened.

32. (Previously presented) The semiconductor testing method according to claim 22, wherein said duration of said test pattern cycle period for said plurality of test patterns is widened successively from the top pattern address throughout the entire test pattern in order.